

Semiconductors 101, unit 15

Process integration: putting hundreds of steps in order

Every step can be done right and the chip still may not work: hundreds of steps have to be put in one flow, and someone has to watch how they affect each other from start to finish.

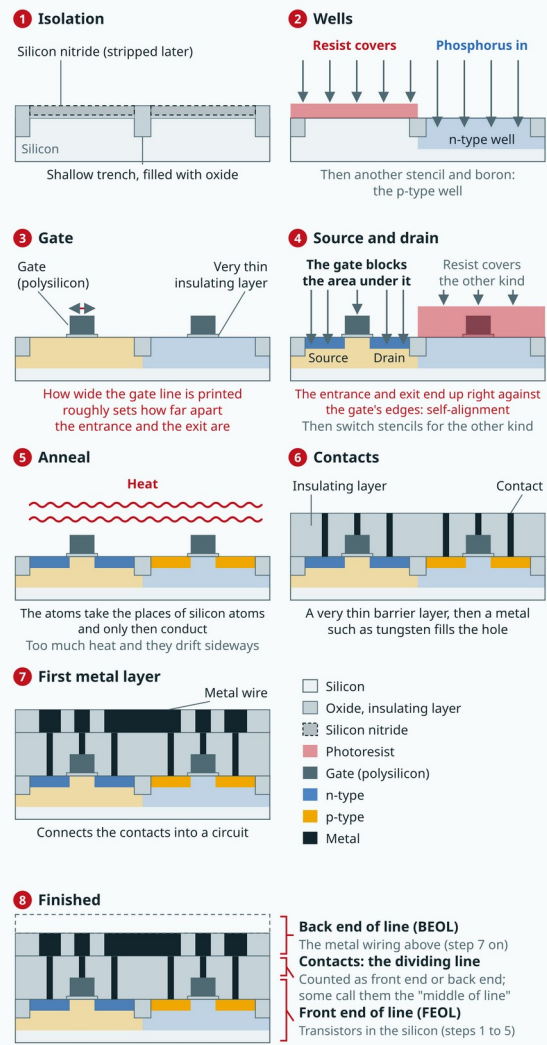
Semiconductors 101: a free course following the life of a chip

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Goals

- 1 Tell in order how one transistor is made (isolation, wells, gate, source and drain, anneal, contacts, the first metal layer) and why each step is needed.
- 2 Explain why the order can't be changed at will (metal can't take high heat, and heat adds up), and why some steps can't wait long between them (Q-time).
- 3 Explain how a chip can come out wrong even when every step is within spec, and how an integration engineer works back from the result.

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A simplified flat transistor, not to scale

Each panel is a cross-section of the same piece of silicon: on the left, the kind of transistor whose entrance and exit are n-type, sitting in a p-type well; on the right, the p-type kind, in an n-type well. A simplified flat transistor, not to scale; the most advanced transistors are

more three-dimensional and take more steps.

Step by step

1 Dig shallow trenches and fill them with oxide to keep each transistor apart (isolation).

Why: Transistors are packed tightly, and each one needs an insulating wall around it.

If not: Neighboring transistors leak into each other, and the switches don't turn off cleanly.

2 Implant phosphorus and boron to make the n-type and p-type wells.

Why: Each kind of transistor sits in one well, its entrance and exit the opposite type from the silicon below, so it stays off.

If not: Without a well of the opposite type, the entrance and exit are connected all the time, and the switch can't turn off.

3 Grow a very thin oxide, lay down polysilicon and print thin gate lines.

Why: The gate controls the channel with its voltage through the insulating layer; how wide it is sets roughly how far apart the entrance and exit are.

If not: An insulating layer too thin leaks and one too thick is slow; a gate too wide is slow and one too narrow doesn't close tightly.

Step by step

4 Use the gate as a shield and implant the source and drain on either side (self-alignment).

Why: A separately printed pattern is always off a little; with the gate as its own shield, they always line up.

If not: Out of line, a gap opens between the entrance or exit and the channel, and current can't get through.

5 Heat the wafer so the atoms settle in (anneal), counting every heating against the thermal budget.

Why: Freshly implanted atoms mostly sit in the wrong spots and don't conduct yet.

If not: Too little heat and the sheet resistance stays high; too much and the atoms drift sideways, blurring the shapes just aligned.

6 Cover with insulator, open small holes and fill them with metal to make the contacts.

Why: The wiring above may touch the transistors only where it should; everywhere else stays insulated.

If not: A hole that stops short of the bottom has high resistance or doesn't conduct at all; one out of line that touches the gate makes a short.

Step by step

7 Put metal on only at the end, making the first metal layer that connects the contacts into a circuit.

Why: Some front-end steps run at over a thousand degrees, and once metal is on, the wafer can't be heated like that again.

If not: Metal first, and the hot steps can no longer be done; left unconnected, the transistors are just separate switches.

Keep them apart, then lay the base: isolation and wells

A fab can't work on just one small patch. To make something happen only in certain places, it first prints a stencil and goes through a full round: grow a film, print the pattern, etch or implant, strip the resist, clean, measure. A chip takes dozens of rounds and hundreds of steps. Taking the simplest, flat transistor, step 1 is isolation: dig shallow trenches into the silicon, fill them with oxide and polish flat, so each transistor has an insulating wall around it; otherwise neighbors leak into each other. Step 2 is the wells: cover half the wafer with resist and implant phosphorus to make the n-type well, then switch stencils and implant boron to make the p-type well. Each kind of transistor sits in one, its entrance and exit the opposite type from the silicon below, and that is what lets it stay off.

Make the gate, then use it as a shield

Step 3 is the gate: grow a very thin oxide as the insulating layer, lay down polysilicon that conducts, and print the gates as thin lines. How wide a gate line is sets roughly how far apart the entrance and the exit are, so it has to be printed especially fine and accurate. Step 4: cover the other kind of transistor with resist and implant atoms on either side of the gate. The gate blocks the area right under it, so the source and drain end up exactly against its two edges; this is self-alignment. (Real flows first do a shallow implant, add thin spacers on both sides of the gate, then do the deep one; that is left out here.) Print a separate pattern to line them up and it will always be off a little, and if that leaves a gap, current can't cross it. Step 5 is the anneal: freshly implanted atoms mostly sit in the wrong spots and don't conduct yet, so the wafer is heated to settle them. Too long, and the atoms drift sideways and blur the shape, so the heat often lasts only seconds.

Once metal goes on, there's no going back

Step 6 is the contacts: cover with a thick insulating layer, polish flat, etch small holes down to the source, drain and gate, lay a barrier layer and fill them with a metal such as tungsten. A hole that stops short of the bottom has high resistance or doesn't conduct at all; one out of line that touches the gate makes a short. Step 7 digs trenches and fills them with metal to make the first metal layer, and only then do the two kinds of switch work as a pair and form a circuit. Steps 1 to 5, which build the transistors, are the front end of line; the wiring is the back end of line. The order has reasons: some front-end steps run at over a thousand degrees, and once metal is on, the wafer can't be heated like that again. Every later heating also moves the atoms implanted earlier a little more, an account called the thermal budget that has to be counted in advance. In production this flow is locked, called the POR.

No long waits between steps, and someone watches the whole line

Between two steps, a wafer sits in a box in the air: cleaned silicon grows back a thin oxide, and developed resist left too long can make the etched line width drift. So a limit is set on how soon the next step must start once one ends, called Q-time; past it, the lot needs rework or even scrap. Steps also affect each other: a film a touch thicker and etch as usual, both within spec, and some contact holes stop just short of the bottom and their resistance goes up. So a process integration engineer (PIE) looks after a product from the first step to the last: every step's measurements, and the electrical results and yield once the wafer is done. When something goes wrong, they work back from the result to find which number moved first.

Common misconceptions

People say: If every step is within spec, the chip is bound to be fine.

In fact: Not necessarily. Steps affect each other: one step drifts a little, the next carries on as usual, each within spec, and together some small holes may not reach the bottom and resistance goes up. So besides each step's measurements, someone has to watch the whole line, including the electrical results and yield once the wafer is done.

People say: A wafer is in the cleanroom, so waiting a bit before the next step does no harm.

In fact: The cleanroom keeps particles out, but not the slow reaction between the surface and the air. Many pairs of steps have a Q-time, and going past it means rework or even scrap. So whoever schedules the lots often thinks in reverse: if the next step isn't ready, don't start the one before it yet.

Play

Play a shift as a process integration engineer: you look after not one tool but a product, from the first step to the last

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Think

- 1 Changing one condition makes this step better but may make a later step worse. Who should have the say over whether to change it? What data should they see before deciding?
- 2 The tool at the next step suddenly stops while a lot's Q-time is counting down. What does waiting for the repair cost, and what does redoing the step before cost?

Read

How is a transistor made? From isolation to the first metal layer, step by step

fab24hr.com/en/blog/transistor-flow/

What does a process integration engineer (PIE) do, and how is it different from a process engineer?

fab24hr.com/en/blog/what-is-pie/

What is Q-time, and why can't wafers wait?

fab24hr.com/en/blog/what-is-q-time/

Semiconductors 101: a free course following the life of a chip

<https://fab24hr.com/en/learn/integration/>

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